ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to an electrostatic discharge protection circuit in a semiconductor integrated circuit.

Description of the Related Art

[0002] Fig. 1 shows an electrostatic discharge (hereinafter abbreviated "ESD") protection circuit constructed with NMOS transistors according to a related art.

[0003] Referring to Fig. 1, a drain of an NMOS transistor N1 is connected to a pad (input or output) 10 and a source is connected to a ground Vss2. A gate is connected to a ground Vss1 when used for an ESD protection circuit or to a pull-down inverter when used for a driving transistor.

[0004] The NMOS transistor N1 includes a parasitic bipolar transistor B1. The parasitic bipolar transistor B1 is constructed with a collector/emitter as the drain/source of the NMOS transistor N1 and a base as a substrate of the NMOS transistor N1. In this case, the base is connected to the ground Vss2.

[0005] The pad 10 is connected to an internal circuit 12 through a resistance R. Between one end of the resistance R and the ground Vss2, an NMOS transistor N2 is located. The NMOS transistor N2 includes another parasitic bipolar transistor of which the gate and

source are connected to each other. In this case, the resistance R reduces an ESD current flowing to the NMOS transistor N2, and the NMOS transistor N2 removes ESD stress still remaining after removal by the NMOS transistor N1.

[0006] Fig. 2 shows a layout of an ESD protection circuit in Fig. 1.

[0007] Operation of the above-constructed ESD protection circuit of the related art is explained as follows.

[0008] Referring to Fig. 2, when ESD stress is applied to the pad, a high voltage is applied to the drain of the NMOS transistor N1. If the high voltage is applied to the drain, holes are discharged to the substrate by junction breakdown between a source region n+ and the substrate p+. In this case, electrons of the source migrate to the drain if the hole current enables a breakdown voltage high enough to overcome a potential barrier of 0.7V between the n+ source region and the p+ substrate. If the potential barrier is overcome, the transistor B1 is turned on, and the required voltage is called a triggering voltage.

[0009] The triggering voltage of the NMOS transistor N1 is about 7V in submicrontechnology. Thus, the triggering voltage becomes higher than the breakdown voltage (~5.5V) of a gate insulating layer of the NMOS transistor. This relationship of the triggering voltage exceeding the breakdown voltage causes damage on the gate insulating layer of the NMOS transistor N1 in the related art.

SUMMARY OF THE INVENTION

[0010] Accordingly, the present invention is directed to an ESD protection circuit that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0011] An object of the present invention is to provide an ESD protection circuit enabling to increase ESD immunity of semiconductor devices.

[0012] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, an ESD protection circuit includes an NMOS transistor connected between an input/output pad and a ground, the NMOS transistor having a parasitic bipolar transistor, and at least one diode connected between the input/output pad and the NMOS transistor.

[0013] In another aspect of the present invention, an ESD protection circuit includes an input/output pad; a plurality of N diodes connected in series between the input/output pad and a substrate of an NMOS transistor wherein the NMOS transistor is connected between the input/output pad and the substrate and has a parasitic bipolar transistor connected to plurality of N the diodes.

[0014] These and other objects of the present application will become more readily apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention and wherein:

[0016] Fig. 1 illustrates an electrostatic discharge protection circuit constructed with NMOS transistors according to a related art;

[0017] Fig. 2 illustrates a layout of the ESD protection circuit in Fig. 1;

[0018] Fig. 3 illustrates an electrostatic discharge protection circuit according to one embodiment of the present invention; and

[0019] Fig. 4 illustrates a layout of the ESD protection circuit in Fig. 3.

DETAILED DESCRIPTION OF THE INVENTION

[0020] Fig. 3 illustrates an electrostatic discharge ESD protection circuit according to a preferred embodiment of the present invention.

[0021] Referring to Fig. 3, in addition to the ESD protection circuit according to the related art, a plurality of diodes D1-Dn are connected between a pad 10 and parasitic bipolar transistor B1. The last diode Dn is connected to a substrate 16 and bipolar transistor B1, as shown in Fig. 4.

[0022] Referring to Fig. 4, a p+ junction of the PN diode D1 is connected to the pad, and an n+ junction of the PN diode D1 is connected to a p+ junction of a second diode D2. Also, an n+ junction of the second diode D2 is connected to a p+ junction of the last

diode Dn. The n+ junction of the last diode Dn is connected to a p-type substrate. The number of diodes connected in series is determined so as to stop the current flow through the diodes on normal operation of a chip.

[0023] Moreover, an output node of diode Dn is connected to a bulk of the NMOS transistor N1, whereby a potential of the substrate (bulk) of the NMOS transistor N1 is controlled by a forward operation of the diode Dn. In this case, the diode Dn is connected between the pad and ground Vss in forward series.

[0024] Although not shown in the figures, the serially-connected diodes may be rearranged to be connected in parallel each other. In this case, the number of diodes utilized is also determined so as to stop the current flow through the diodes on the normal operation of a chip.

[0025] As shown in Fig. 3, the drain of the NMOS transistor N1 is connected to the pad 10 (input or output pad), the source is connected to the ground Vss2, and the gate is connected to Vss1 or a pull-down inverter. The parasitic bipolar transistor B1 is connected to the diodes D1-Dn and the ground Vss2. The diodes D1-Dn are connected to the base of the bipolar transistor B1. The bipolar transistor B1 provides a base of the NMOS transistor N1. In this case, 'Rsub,' as shown in Figure 3, is a substrate resistance.

[0026] Operation of the above-constructed ESD protection circuit according to the present invention is explained as follows.

[0027] When ESD stress is applied to the pad 10, high voltage is applied to both the drain of the NMOS transistor N1 and the diode D1. In this case, the corresponding diode D1 becomes turned on if the voltage becomes equal to or higher than about 0.7V, which is a

built-in voltage of a PN junction, since the diodes are connected to each other in a forward direction. As is well known in the art the built-in voltage of the PN junction may vary.

[0028] Yet, as the present diodes are connected in series, a voltage of the node A is dropped down by an amount (number of diodes Dn x 0.7V) so as to be applied to the substrate. For instance, if 5 diodes are connected in series to each other, a voltage at a node B becomes the voltage attained by subtracting 3.5V from the voltage at node A. Once the voltage over 3.5V is applied to the pad, all the diodes are turned on so as to increase a potential of the substrate. If the potential of the substrate becomes high, a voltage drop (for example, 0.7V) occurs with ease between the source of the bipolar transistor B1 and substrate. Thus, the triggering voltage of the bipolar transistor B1 is reduced.

[0029] As a result, a triggering of the bipolar transistor B1 may occur even at a low voltage. If the bipolar transistor B1 is turned on at the low voltage, a voltage applied to the NMOS transistor N1 and its gate insulating layer is reduced. Thus, the influence or damage to the gate insulating layer of the NMOS transistor N1 is decreased.

[0030] Moreover, when measured by applying a voltage to the substrate of the NMOS transistor N1 in the manner of the present invention, a second breakdown current (It2 value) representing ESD performance becomes even higher.

[0031] As mentioned in the above description, the present invention improves ESD performance by turning on the parasitic bipolar transistor of the NMOS transistor at a voltage lower than that of the conventional art.

[0032] Accordingly, the present invention allows the prevention of a gate insulating layer from receiving a high voltage by turning on a protection circuit at a lower

voltage so as to shunt the ESD current as well as improve ESD performance by increasing a magnitude of It2.

[0033] The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.